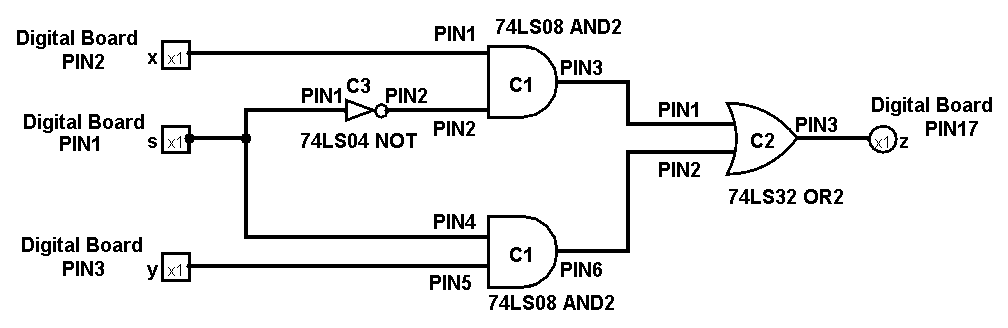
**CSC258 – Lab1 Ruijie Sun & Xin Luo**

**Part 1: 1003326046 & 1003069706**

**Function**: *f = xs’ + ys*

**Chips used:**

C1 – 74LS08 AND gate

C2 – 74LS32 OR gate

C3 – 74LS04 NOT gate

**Connected to all chips:**

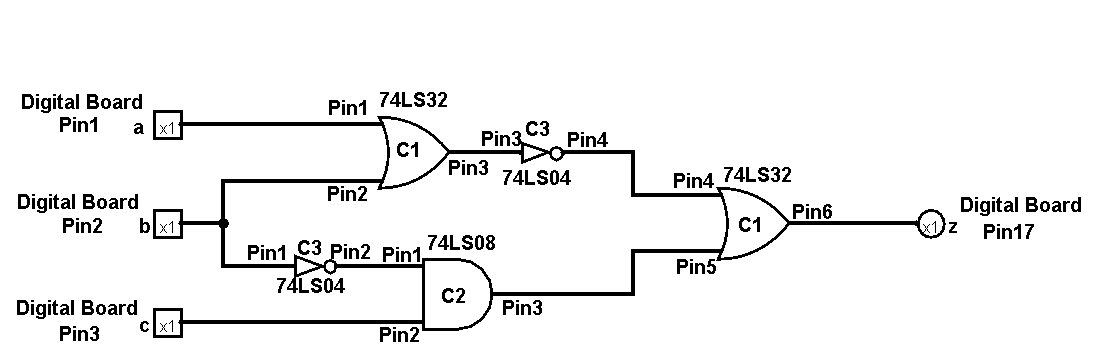
PIN#7 – Gnd

PIN#14 – Vcc

**Truth Table** :

|  |  |  |  |
| --- | --- | --- | --- |
| S | X | Y | Z |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

**Part 2:**

**Function**: *f = (a+b)’ + cb’*

**Chip used:**

C1 - 74LS32 OR gate

C2 - 74LS08 AND gate

C3 - 74LS04 NOT gate

**Connected to all chips:**

PIN#7 – Gnd

PIN#14 – Vcc

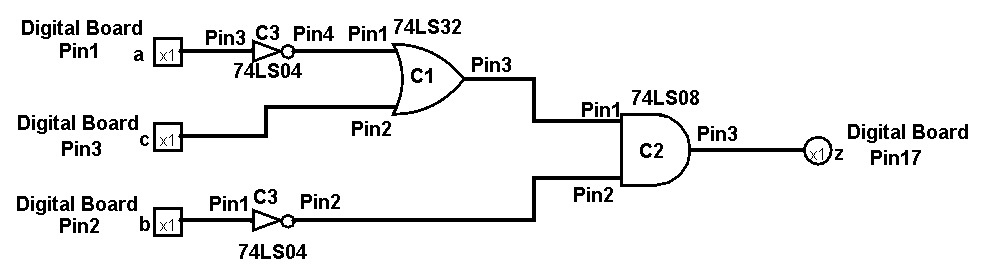
**Truth Table**:

|  |  |  |  |
| --- | --- | --- | --- |
| a | b | c | z |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 |

**Improved function:**

*f = (a+b)’ + cb’* As I shown in the two schematic Diagrams, the

*= a’b’ + cb’* number of gates used reduced to 4 from 5.

 *= b’(a’ + c)*

**Chip used:**

C1 - 74LS32 OR gate

C2 - 74LS08 AND gate

C3 - 74LS04 NOT gate

**Connected to all chips:**

PIN#7 – Gnd

PIN#14 – Vcc

**Truth Table (same as before) :**

|  |  |  |  |
| --- | --- | --- | --- |
| a | b | c | z |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 |